AMENDMENTS TO THE CLAIMS

Claims 1-14: (cancelled)

Claim 15 (new): A memory accessing system for achieving increased memory capacity of a microprocessor, the memory accessing system comprising:

an external memory including a single physical region; and

an address translator coupled between the microprocessor and the external memory for translating a page and an address within the page pointed to by the microprocessor when accessing the external memory into a physical address of the external memory, and for mapping a predetermined range of addresses within all pages pointed to by the microprocessor when accessing the external memory into the single physical region of the external memory.

Claim 16 (new): The memory accessing system of 15, wherein the predetermined range of addresses within all pages is relatively the same range of addresses within all pages.

Claim 17 (new): The memory accessing system of claim 15, wherein the address translator is further for mapping addresses outside the predetermined range of addresses within all pages to areas of the external memory not within the single physical region.

Claim 18 (new): The memory accessing system of claim 15, wherein the external memory further includes a plurality of non-common areas, each page to which the microprocessor can point when accessing the external memory having a corresponding non-common area within the external memory.

Claim 19 (new): The memory accessing system of claim 18, wherein the address translator is further for mapping addresses outside the predetermined range of addresses for each page to a physical address of the external memory being within

a non-common area corresponding to the page being pointed to by the microprocessor.

Claim 20 (new): The memory accessing system of claim of 15, wherein the address translator comprises:

a multiplier coupled to page select lines of the multiprocessor for multiplying a page number pointed to by the multiprocessor when accessing the external memory by a non-common area size to thereby generate an offset value;

a comparator coupled to address lines of the multiprocessor for comparing an address within the page pointed to by the multiprocessor when accessing the external memory with a size of the single physical region to thereby generate a select signal, the select signal being asserted if the address within the page pointed to by the multiprocessor is less than the size of the single physical region;

an adder coupled to address lines of the multiprocessor and the multiplier for adding the address within the page pointed to by the multiprocessor and the offset value to thereby generate a non-common data physical address value; and

a multiplexer coupled to the address lines of the multiprocessor, the adder, and the comparator for outputting the physical address of the external memory as the non-common data physical address value when the select signal is not asserted, and for outputting the physical address of the external memory as the address within the page pointed to by the multiprocessor when the select signal is asserted.

Claim 21 (new): The memory accessing system of claim of 20, further comprising a programmable register for storing the size of the single physical region.

Claim 22 (new): A method of memory access for achieving increased memory capacity of a microprocessor, the method comprising:

providing an external memory including a single physical region;

translating a page and an address within the page pointed to by the microprocessor when accessing the external memory into a physical address of the external memory; and

mapping a predetermined range of addresses within all pages pointed to by the microprocessor when accessing the external memory into the single physical region of the external memory.

Claim 23 (new): The method of 22, wherein the predetermined range of addresses within all pages is relatively the same range of addresses within all pages.

Claim 24 (new): The method of claim 22, further comprising mapping addresses outside the predetermined range of addresses within all pages to areas of the external memory not within the single physical region.

Claim 25 (new): The method of claim 22, wherein the external memory further includes a plurality of non-common areas, each page to which the microprocessor can point when accessing the external memory having a corresponding non-common area within the external memory.

Claim 26 (new): The method of claim 26, further comprising mapping addresses outside the predetermined range of addresses for each page to a physical address of the external memory being within a non-common area corresponding to the page being pointed to by the microprocessor.

Claim 27 (new): The method of claim of 22, further comprising:

multiplying a page number pointed to by the multiprocessor when accessing the external memory by a non-common area size to thereby generate an offset value;

comparing an address within the page pointed to by the multiprocessor when accessing the external memory with a size of the single physical region to thereby generate a select signal, the select signal being asserted if the address within the

page pointed to by the multiprocessor is less than the size of the single physical region;

adding the address within the page pointed to by the multiprocessor and the offset value to thereby generate a non-common data physical address value; and

outputting the non-common data physical address value as the physical address of the external memory when the select signal is not asserted, and outputting the address within the page pointed to by the multiprocessor as the physical address of the external memory when the select signal is asserted.

Claim 28 (new): The method of claim of 27, further comprising storing the size of the single physical region in a programmable register.